Auto-zero stabilized CMOS amplifiers for very low voltage or current offset

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Abstract---In this paper, we present two amplifiers designed in CMOS technology and including an auto-zero architecture for very low offset control. The first design is a high precision operational amplifier focusing on the voltage offset. It is a continuous time auto-zero stabilized architecture, that leads to a typical input offset voltage of 2µV-100nV/°C. The amplifier with its output buffer consumes 5mW at a supply voltage of +/- 2.5V. The gain bandwidth product is 2MHz while the slew rate is respectively -6V/µs and +8.8V/µs on 10pF with 10KΩ load. This amplifier is suitable for the control of large dynamic (>10^5) calibration signal, and for very low DC signal instrumentation.

The second design is a current mode charge pulse amplifier based on a second generation positive current conveyor topology (CCII). The bandwidth, the dynamic range and the output impedance have been optimized using an enhanced cascode current mirror. The preamplifier provides two outputs: one for the signal integration, and another going through a current comparator for a digital counting flow. The double hit resolution is less than 7ns. An auto-zero compensation has been added to this preamplifier to control its output current offset down to 60nA. The total power dissipation (preamplifier + offset cancelation + comparator) is less than 1mW. This second amplifier has been designed for low power space applications, especially EUSO (Extreme Universe Space Observatory), which use multianode PMT in the configuration of a large gate time (2.5µs) open for charge integration.

I. Introduction.

Voltage offset is a very important parameter for operational amplifiers used in many applications: calibration signal for high energy physics, low signal sensor interfaces, high accuracy instrumentation. In the same way, current offset is crucial for current conveyor amplifiers used in an integrator configuration.

Auto-zero stabilization architecture is an efficient and elegant solution for offset cancellation. Also it helps to compensate the offset drift (with the time, temperature, power supply etc.). Some other advantages of autozero amplifiers include the possibility to feature a high open loop gain and a high CMRR/PSRR. CMOS technology is suitable for such a design, due to its analog switch capabilities, lower power architectures and low cost.

This auto-zero concept has been adapted and simplified for a low power current conveyor preamplifier designed for the EUSO experiment analog front-end. The output current offset is crucial for this application because it is continuously integrated on the output capacitor with the signal pulses, over a long time of 2.5µs so called Gate Time Unit (GTU). Hence the output signal is: $(I_{offset}+\delta I_{signal})*GTU/C_{out}$. The power dissipation is a very important parameter for this space application, therefore the offset cancellation loop must consume a very low current. This circuit has been designed in a 0.35µm CMOS process.

A brief review of the auto-zero concept is given in section II. The design and the results of the low voltage offset amplifiers are presented in section III. The low current offset amplifier design and testing results are given in section IV.

II. Auto-zero amplifier: Overview.

A continuous time auto-zero amplifier requires two internal amplifiers [1]. The so called 'Main amplifier' is unswitched and continuously available for the incoming signal amplification (Figure 1).

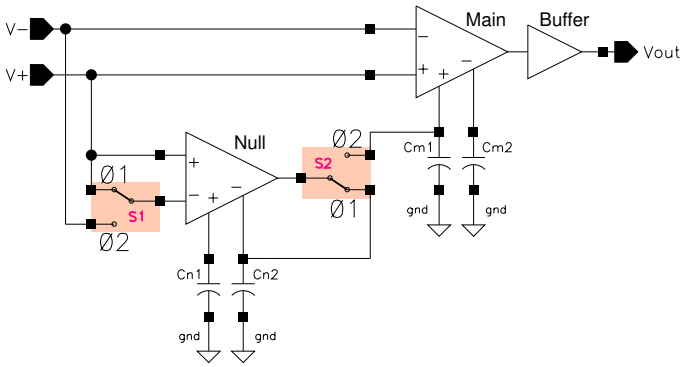


Figure 1 Auto-zero amplifier block diagram

The offset cancellation consists of two alternating successive phases. During the first one, the 'Nulling amplifier' is disconnected from the signal path for its own auto correction. A correction signal V_{cn} is generated and held on capacitors C_n connected at the auxiliary inputs.

During the second phase, the Nulling amplifier is reconnected to the Main one and senses its inputs offset. Another correction voltage V_{cm} is generated this way and held on capacitor C_m for the Main amplifier correction.

Each internal amplifier (the Nulling and the Main) could be modelized with two differential inputs: a primary and an auxiliary one as shown in Figure 2.

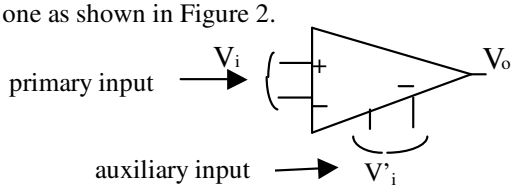


Figure 2: Internal amplifier model

From this model can be made the assumption that the primary and auxiliary inputs are combined in the first stage of the amplifier, leading to an output signal $V_0(s)$ expressed as:

$$V_o(s)=A(s).V_i+A'(s).V'_i+A(s).V_{os} \quad (1)$$

where V_{os} is the offset voltage in the primary input of the amplifier.

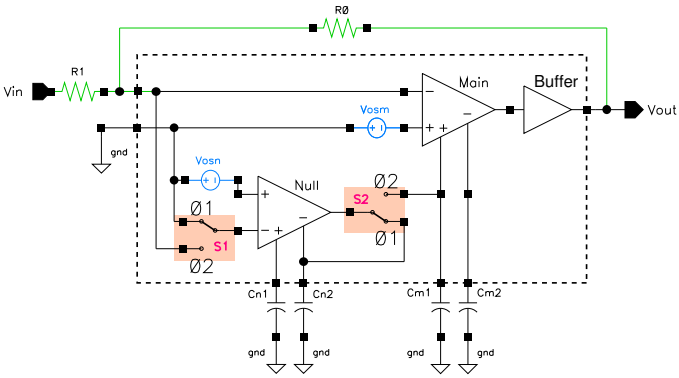


Figure 3: Auto-zero amplifier in feedback loop

Consider now the full auto-zero amplifier in a feedback loop configuration as shown in figure 3. V_{osm} and V_{osn} are respectively the inherent offset of the Main and the Nulling internal amplifiers. ΔV_{cm} and ΔV_{cn} are the perturbation voltages respectively on the capacitors C_m and C_n, related to the charge injection, sampling noise and leakage current .

During the phase ϕ_1, the switch S_1 short-circuits the Nulling amplifier, then its output stores a control voltage V_{cn} on the capacitor C_n through the switch S_2. During the following phase ϕ_2, the Null amplifier senses the offset of the Main and stores the resulting control voltage V_{cm} on the capacitor C_m. After many successive iterations of ϕ_1 and ϕ_2 phases, the offset will decrease step by step.

Let α be the constant ratio between the open loop gains:

$$\alpha_m = A_m/A'_m \text{ and } \alpha_n = A_n/A'_n \quad (2)$$

One can demonstrate [2] that the maximum value of the residual offset at the Main amplifier input is:

$$V_{os}^{\max} = \frac{(\alpha_m/\alpha_n)V_{os_m}^{\max} + V_{os_n}^{\max}}{A'_n} + \frac{\Delta V_{c_m}}{\alpha_m} + \frac{\Delta V_{c_n}}{\alpha_n} \quad (3)$$

If the same architecture is used for the Main and the Null amplifier, then $\alpha_m=\alpha_n=\alpha$ and $A_n=A'_n$; so $V_{os}^{\max}$ becomes:

$$V_{os}^{\max} = \frac{V_{os_m}^{\max} + V_{os_n}^{\max}}{A'} + \frac{\Delta V_{c_m}}{\alpha} + \frac{\Delta V_{c_n}}{\alpha} \quad (4)$$

This voltage offset could be minimized with a large value for the auxiliary inputs open loop gain A', (more than 40dB). Moreover, the sensitivity to the fluctuation voltage ΔV over the capacitors C_m and C_n can be limited by using an internal amplifier architecture that leads to a large value of the α ratio, and by using also external large capacitance.

III. INTERNAL AMPLIFIER FOR THE VOLTAGE OFFSET AUTO-ZERO AMPLIFIER

A. Architecture

The diagram shown in figure 4 is used for both internal amplifiers (the Main and the Null). Its general architecture is the folded cascode, to provide a high open loop dc gain and the capability to drive a large hold capacitor. A high-swing current mirror is used in the cascode amplification stage (M_7-M_{10}) to improve the bandwidth and the outpout dynamic range, [3]. The high-swing current mirror will be described in detail in section IV-B.

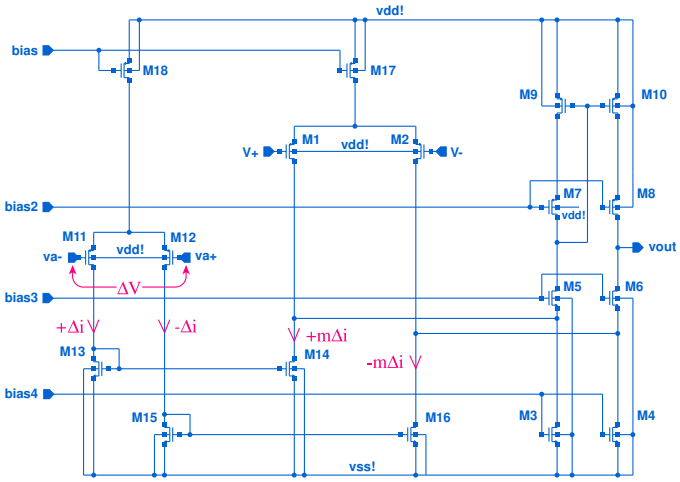


Figure. 4. Internal amplifier diagram

The offset depends mainly on how the quiescent current is well balanced through the primary differential input stage. This equilibrium is controlled from the auxiliary inputs (V_a+, V_a). An offset control signal ΔV at the auxiliary inputs will generate a fluctuation current Δi around the quiescent point in the long tail auxiliary amplifier. Then the current miror (M13,M14), respectively (M15,M16) will create a control current +/-mΔi in the primary stage which after the amplification stage will lead into an offset change ΔV_0 after the cascode stage.

From figure 4, one can write two equations for ΔV_0:

$$\Delta V_0 = (m*\Delta i)/g_m*A = (m * g_{m'} *\Delta V)/g_m * A; \text{ and } \Delta V_0=A'*\Delta V$$

Therefore in this configuration the α parameter is:

$$\alpha = g_m/(m*g_{m'})$$

where g_m and g'_m are respectively the transconductance for the primary and auxiliary input pairs.

An output buffer (common source output stage not described here) has been added after the Main amplifier output to enhance its driving capability for resistive loads.

The simulation results in figure 5 demonstrate how in a feedback configuration (as in figure 1), the compensation is performed step by step until the voltage offset seen at the output is closed to the noise. An input basic offset of -10mV (and respectively +10mV) was taken as worst case assumption for the Main and Null amplifiers before the compensation

starts. The feedback loop gain is R0/R1=100, and the sampling frequency is 100Hz.

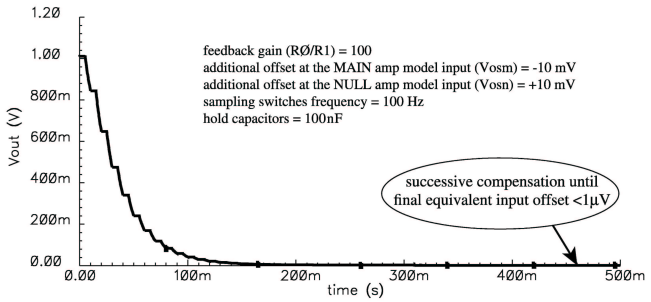


Figure 5: Voltage offset compensation step by step

B. Experimental results

This amplifier has been designed in a standard 0.8µm process, and 5 prototypes have been tested. The mean value found for the offset is less than 2µV at home temperature. An evaluation of a typical offset drift with the temperature is shown in figure 6. Neither the min nor the max characteristics are linear. But from the fitting curve a mean value for the drift around 100nV/°C can be noticed.

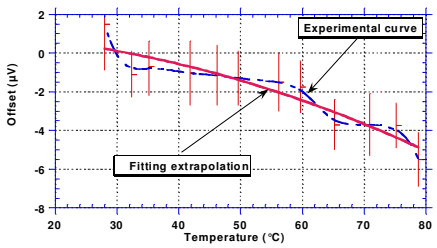


Figure 6: Offset drift with the temperature.

The output impedance of the main amplifier's buffer was measured to be around 400 Ohms. The open loop gain (from the primary inputs to the buffer output) is better than 100dB. The gain bandwidth product is 2MHz while the slew rate is respectively -6V/µs and +8.8V/µs on 10pF with 10KΩ load.

Figure 7 shows the equivalent input noise voltage spectrum measured while the total power dissipation was set at 5mW (including the output buffer), and the supply voltage was +/- 2.5V. an input noise voltage of 10nV/√Hz beyond 30Khz can be seen.

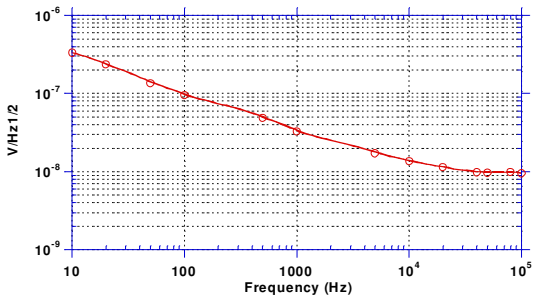


Figure 7: Equivalent input noise voltage

IV. CURRENT CONVEYOR AMPLIFIER WITH A CURRENT OFFSET AUTO-ZERO LOOP

The following section describes a second design where an auto-zero architecture is used.

Current conveyor preamplifiers have been successfully used for many physics applications [4] [5] [6] where low noise, low power and high speed were the main concern. In recent CMOS processes the low supply voltage becomes a further critical parameter for the dynamic range. The EUSO experiment uses a multianode PMT and the front-end electronics includes a digital flow for photon counting, and an analog charge integrator flow. So a current conveyor preamplifier appears to be a good compromise. The output stage consists of two current mirrors: one going to a current comparator for the counting flow, and the second one loaded by a capacitor for the output current integration (see figure 9). Over and above the low power consumption, the main features of this electronics are the time double hit resolution (for the counting flow), the current offset and the dynamic range (for the analog flow).

A. The current offset auto-zero loop

There is a short reset time (40ns) after each GTU integration time (2.5µs). During the GTU, the preamplifier is disconnected from the auto-zero loop, letting the base line constant. During each reset time the preamplifier is disconnected from the output capacitor, and then connected to another capacitor where the output current offset is integrated. The resulting signal is applied to one input of a low gain long tail amplifier which generates the offset control signal that will be sampled and stored on the gate of a transistor. The current flowing through this transistor comes in parallel with the bias current of the preamplifier's output stage. Therefore we have an offset cancellation loop which is a controlled and sampled current copier in parallel with the main bias current [7].

Figure 8 shows some simulation results: the first curve is the current offset through the output capacitor. During each reset time (40ns) the auto zero loop controls this offset, and step by step reduces it down to a few nA. The second curve is the sampled control signal going on the gate of the transisors which will induce the offset cancellation current.

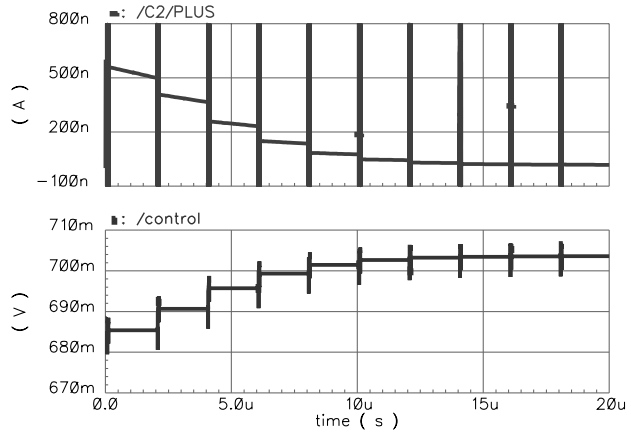


Figure 8: Current offset cancellation and its control signal

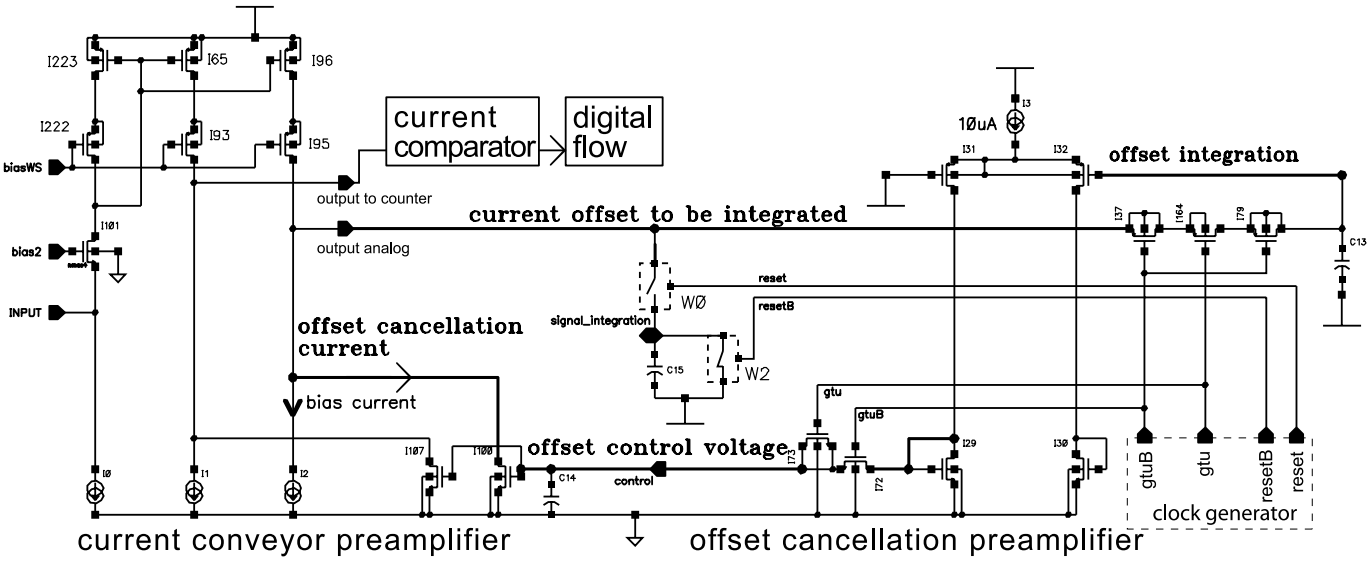
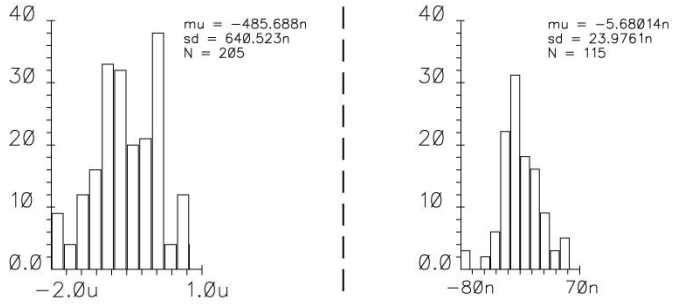


Figure 9: Current preamplifier with the offset cancellation loop

The offset Monte Carlo simulations are shown in figure 10 for the preamplifier without and with the auto-zero loop.



(a) basic current conveyor offset; (b) with the auto-zero loop

Figure 10: Current offset Monte Carlo simulations

Over the process mismatch we could expect an output current offset spread from only -80nA to +70nA, instead of -2uA to 1uA found in the configuration without the auto-zero loop in spite of using transistors with twice the minimum channel length [8]. The differential pair (figure 9) is biased with only 10µA to save power consumption, and a great care was taken in the layout to limit its own offset. The logic signals (reset, resetB, gtu, gtuB) come from a no overlapping clock generator cell integrated inside the chip. The sequences and the edge of these signals controlling the CMOS switches are carefully defined to limit the charge injection.

This circuit has been designed in a .35µm CMOS process. The offset testing results statistics over a set of 10 prototypes are shown in figure 11.

It turns out that with the exception of one chip which has an offset of 150nA, this first prototypes set has an offset dispersion from –50nA to 60nA. It is very close to the Monte Carlo simulations of figure 10 (b), and confirms the efficiency of the auto-zero loop.

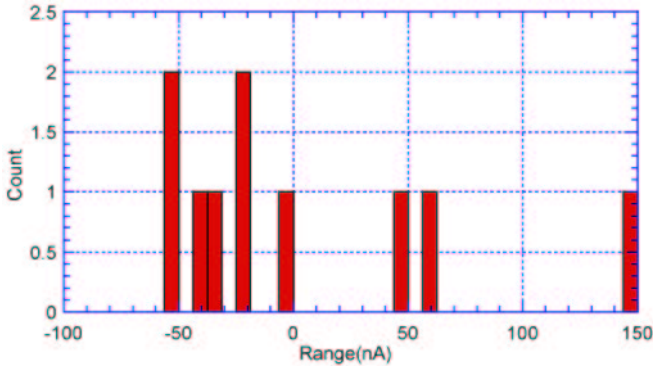


Figure 11: current offset dispersion over 10 prototypes

B. The wide swing current mirror

The current conveyor of figure 9 and the amplifier described in figure 4 use both a current mirror architecture so called “wide swing mirror” [9][10]. It is shown in figure 12(b), beside the classical cascode.

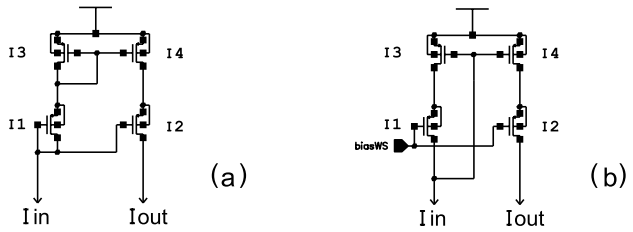


Figure 12: Classical cascode (a) and wide swing current mirror (b)

The cascode architecture is an easy way to increase the output impedance of a current mirror, and thus to improve the output current accuracy over the dynamic range. For both architectures, the output impedance is:

$$Ro = (\delta I_{out}/\delta V_{out})^{-1} = Ro_{(I2)} + Ro_{(I4)} + g_{m(I2)} * Ro_{(I2)} * Ro_{(I4)}$$

$$\approx g_{m(I2)} * Ro_{(I2)} * Ro_{(I4)}$$

Figure 13 shows how long this output impedance is quite constant, and also points at the difference of dynamic range[]. For transistors of equivalent size, and with saturation condition for each one ($V_{ds}>V_{gs}-V_t$), it can be demonstrated that the minimum voltage drop for the basic cascode is:

$V_{out}=V_t + 2V_{dssat}$

In the case of high swing structure, a careful choice of the bias voltage could lead into a voltage drop of $Vout=2V_{dssat}$. That makes a difference of one V_t , which is confirmed also by the simulations of figure 13.

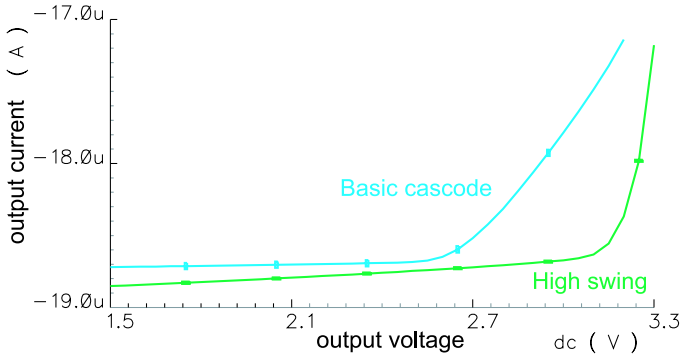


Figure 13: Current mirror dynamic range improvement

In the same way, a suitable choice for the size of transitors I_1 and I_2, helps in improving the bandwidth as shown in figure14. Consequently, the photon double hit time resolution was found less than 7ns.

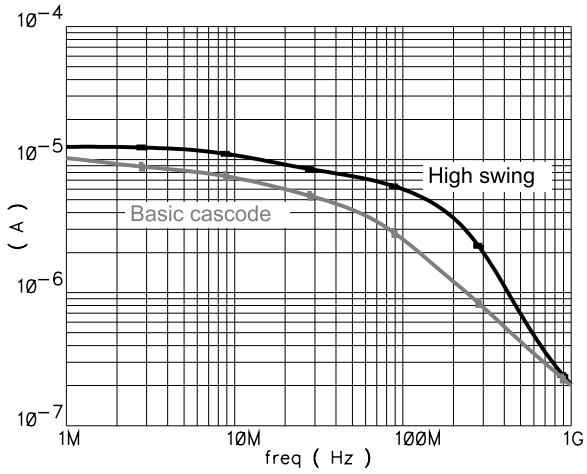


Figure 14:Bandwidth improvement for current mirrors

V. CONCLUSION

Two amplifiers including an auto-zero loop have been successfully designed and tested. The continuous time offset cancellation loop is described for both voltage and current offset. The first prototypes results are presented and show a real efficiency of the auto-zero loop. The high swing current mirror used in the both amplifiers also described. It was very helpful for the dynamic range and the bandwidth, especially for the current amplifier where the low voltage and low power constraints were critical.

ACKNOWLEDGEMENT

The authors would like to thank their colleague G. Boson and J.P. Richer for helpful discussions.

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This work was supported in part by ‘Le Programme d’Actions Intégrées Franco-marocain PAI MA/01/05 ’.